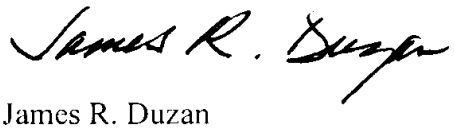
REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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Enclosures: Version of Specification with Markings to Show Changes Made
Version of Claims with Markings to Show Changes Made

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Please replace Paragraph **[0003]** as follows:

[0003] State of the Art: Dynamic random access memory, otherwise known as a DRAM memory chip, die, or device, is a popular type of semiconductor memory device. A DRAM memory device is essentially multiple arrays formed by a series of memory cells including a transistor, such as a metal oxide semiconductor field effect transistor ([MOFSET]MOSFET) and an associated capacitor connected thereto fabricated on a substrate, such as a silicon substrate. The memory cells are combined with peripheral circuits to form the DRAM device. The state of the memory cell, either charged or uncharged, represents the state of a binary storage element, zero or one, (data) stored by the DRAM device in the memory cell. Multiple capacitors on a single silicon substrate or chip are therefore capable of storing large amounts of data. The greater the number of capacitors formed on a substrate or chip, the greater the memory capabilities of the DRAM memory device.

Please replace Paragraph **[0009]** as follows:

[0009] Alternating layers of Ge-BPSG and BPSG, or NSG, are deposited on electrical contacts of a DRAM memory device or [Metal Oxide Semiconductor Field Effect Transistor]metal oxide semiconductor field effect transistor (MOSFET) using chemical vapor deposition (CVD) processes or plasma enhanced chemical vapor deposition processes (PECVD) using suitable apparatus operating at either atmospheric pressure levels or sub-atmospheric pressure levels. The layers are deposited in clusters such that individual capacitance cells are formed having trenches or spaces between each capacitance cell. Once the desired capacitance cell thickness is reached, the capacitance cells are capped with an etch-resistant layer. Introduction of either a wet or dry etchant into the trenches between the capacitance cells, however, etches the alternating layers at varying rates, thereby forming the rippled or corrugated wall of each capacitor cell. The form of the rippled or corrugated configuration of the capacitor

cell wall is dependent upon the etch rates of the alternating layers, and specifically on the concentration of germanium (Ge) in the Ge-BPSG layers forming the capacitor cell.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A semiconductor device comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of [the]said at least one layer of boro-phospho silicate glass.

3. (Amended) A semiconductor device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

4. (Amended) A semiconductor memory device comprising:

at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of [the]said at least one layer of boro-phospho silicate glass.

6. (Amended) A semiconductor memory device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

7. (Amended) A semiconductor memory device comprising:

at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of [the]said at least one layer of boro-phospho silicate glass.

10. (Amended) The memory device of claim 9, further comprising:

at least one dielectric layer; and

a conductive layer over [the]said at least one dielectric layer.

11. (Amended) The memory device of claim 10, wherein [the]said at least one dielectric layer comprises one of Si_3N_4, Ta_2O_5, [and]or BST.

12. (Amended) The memory device of claim 10, wherein [the]said conductive layer comprises Si-Ge.

13. (Amended) The memory device of claim 9, further comprising:

at least one dielectric layer covering at least portions of [the]said plurality of layers of boro-phospho silicate glass and [the]said plurality of layers of germanium boro-phospho silicate glass; and

a conductive layer covering at least a portion of [the]said at least one dielectric layer.